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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/775,070	PARK ET AL.
	Examiner	Art Unit
	Tu-Tu Ho	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/30/2004 is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-4, 6-9, 12-14, and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by Nuxoll et al. U.S. Patent 6,307,769 (the '769 patent).

The '769 patent discloses in Figures 3A-3B and respective portions of the specification an array printed circuit board as claimed.

Referring to **claim 1**, the reference discloses an array printed circuit board, comprising:

at least one circuit board (31) having a first surface, a first layout of first and second chip mounting regions formed on a first half of the first surface (the layout comprising chips 33/35/33 of the, for example, left upper side of Fig. 3B) and a second layout of first and second chip mounting regions formed on a second half of the first surface (the layout comprising chips 35/33/35 of the right upper side of Fig. 3B), the first and second layouts having opposite first and

second chip mounting region patterns (it is apparent that layout 33/35/33 and layout 35/33/35 having opposite first and second chip mounting region patterns).

Referring to **claim 12** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the reference discloses an array printed circuit board, comprising:

at least one circuit board having a front and rear surface, the front surface having a first pattern of first and second chip mounting regions (the pattern comprising chips 33/35/33..35, Fig. 3B) and the rear surface having a second pattern of first and second chip mount regions (the pattern comprising chips 35/33/35..33, Fig. 3B), the second pattern being an opposite of the first pattern.

Referring to **claim 6** and using the same reference characters, citations, and interpretations as detailed above for claims 1 and 12 where applicable, the reference further discloses that the circuit board has a second surface opposite the first surface, the second surface has a first half disposed under the first half of the first surface and a second half disposed under the second half of the first surface, the second layout formed on the first half of the second surface and the first layout formed on the second half of the second surface.

Referring to **claims 2 and 7**, the reference further discloses that the first layout (layout 33/35/33) provides for alternating first (33) and second chip (35) mounting regions beginning with the first chip (33) mounting region and the second layout (35/33/35) provides for alternating first and second chip mounting regions beginning with the second chip (35) mounting region.

Referring to **claim 13**, the reference further discloses that the first pattern provides for alternating first and second chip mounting regions beginning with the first chip (33) mounting

region and the second pattern provides for alternating first and second chip mounting regions beginning with the second chip (35) mounting region.

Referring to **claims 3-4, 8-9, 14, and 16**, the reference further discloses that the first chip (33) and the second chip (35) can be different in type and size (column 10, lines 56-59), thereby disclosing that the first and second chip mounting regions have different layouts.

3. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Yoda et al. Japanese Patent 9-223856 (the '856 patent, cited by Applicant).

The '856 patent discloses in the figures, particularly Figure 3, an array printed circuit board, comprising:

at least one circuit board (20) having a first surface, a first layout of first and second chip mounting regions formed on a first half of the first surface (first layout is generally defined by the left haft region of Fig. 3 and comprising regions 10 having pattern A) and a second layout of first and second chip mounting regions formed on a second half of the first surface (second layout is generally defined by the right haft region of Fig. 3 and comprising regions 10 having pattern B), the first and second layouts having opposite first and second chip mounting region patterns (as is evident form Fig. 3).

4. **Claims 12 and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshihara et al. Japanese Patent 10-150295 (the '295 patent, cited by Applicant).

The '295 patent discloses in the figures, particularly Fig. 1, and the (translated) Abstract an array printed circuit board, comprising:

at least one circuit board (5) having a front and rear surface, the front surface having a first pattern ((F) and (A)) of first and second chip mounting regions and the rear surface having a second pattern ((A) and (F)) of first and second chip mount regions, the second pattern being an opposite of the first pattern.

Referring to **claim 16**, it is apparent that the first and second chip mounting regions have different layouts.

Claim Rejections - 35 USC § 102 or 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1 and 4 are** rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Yoshihara et al. Japanese Patent 10-150295 (the '295 patent, cited by Applicant).

The '295 patent discloses in the figures, particularly Fig. 1, and the (translated) Abstract an array printed circuit board as claimed or substantially as claimed.

Referring to **claim 1**, the reference discloses an array printed circuit board, comprising:

at least one circuit board (5) having a first surface, a first layout (F, Figs. 1 and 2) of a chip mounting region formed on a first half of the first surface and a second layout (reverse F or A) of a chip mounting region formed on a second half of the first surface, the first and second

layouts having opposite first and second chip mounting region patterns (as is apparent from Fig. 2 or from the disclosure in the Solution Section of the Abstract). However, the reference does not appear to disclose that each of the first and second layouts comprises first and second chip mounting regions as claimed. Nevertheless, the missing limitation is either: (1) inherent because Fig. 7 appears to depict first and second chip mounting regions for each of the first and second layouts, or: (2) obvious to one or ordinary skill in the art ("the artisan") because the artisan would easily recognize that each of the first and second layouts was not restricted to just one chip, hence the artisan would populate each of the first and second layouts with a plurality of chips, if the need arises, so as to avoid using another printed circuit board, and so that each of the first and second layouts comprises first and second chip mounting regions.

Referring to **claim 4**, it appears that the first and second chip mounting regions depicted in Fig. 7 have different layouts.

Claim Rejections - 35 USC § 103

6. **Claims 5, 10-11, 15, and 17** are rejected under 35 U.S.C. §103(a) as being unpatentable over Nuxoll et al. U.S. Patent 6,307,769 (the '769 patent) in view of Nakano U.S. Patent 4,733,461.

The '769 patent discloses an array printed circuit board as claimed and as detailed about but fails to disclose that a number of such boards could be sequentially connected to one another. In particular, the reference fails to disclose that a number of the circuit boards are sequentially connected to one another in a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board.

Nakano, in disclosing an array printed circuit board, teaches that in order to increase capacity for an integrated circuit (IC), many chips are attached to a printed circuit board, and to further increase the capacity, a number of printed circuit boards are staked together (column 1, lines 12-25). In other words, per the teachings of Nakano, to further increase capacity of IC's, one would form an IC such that a number of the circuit boards are sequentially connected to one another. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '769 patent's array printed circuit board such that a number of the circuit boards are sequentially connected to one another. One would have been motivated to make such a change to increase the capacity of the device that the circuit board constitutes, as taught by Nakano, and the array printed circuit board such modified would also comprises the limitation "in a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board".

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
April 21, 2005